

Paralleling of HDM Series DC-DC Converters

General Description

Paralleling of Rantec DC-DC Converters for increased power output is accomplished by connecting the inputs, outputs, and sense lines in parallel, with one additional connection made between the parallel control pins. The connection between parallel control pins forces the modules to share the load current within a few percent.

Parallel Signal

The signal at the parallel control pins, shared by parallel-connected modules, is a DC signal that varies between about zero and six volts, depending on input line voltage and output loading. The signal is referenced to $-V_{in}$ on the HDM+ and HDM series converters. The signal is referenced to $-Sense$ on the HDM-200 series converters. The signal is sensitive to both conducted and radiated noise, as well as transient voltages.

Layout Considerations

Best results are obtained by implementing the following practical considerations in making a layout for paralleled modules, in order to keep the input, output and parallel signals as noise-free as possible.

All of the minus input pins of the paralleled modules should be kept at as near the same potential as possible, preferably by a large plane-type connection of a printed circuit board. The input DC current and input ripple currents flow in this connection and can induce noise on, as well as cause level shifting of the parallel control signal in the HDM and HDM+ series converters, resulting in unequal voltages appearing at the individual parallel control pins of the connected modules. For this reason, the connection should be physically as large as possible. A capacitor placed across the input pins

(from $+V_{in}$ to $-V_{in}$) of each paralleled module will reduce the ripple current in the minus input connection and improve paralleled performance. A ceramic capacitor, about 0.1 μ F to 0.47 μ F is suggested. The capacitor should be physically located as close to the converter's pins as possible.

The parallel control pin connection may be very small, as negligible currents flow between the modules. The placement of the connection is important, as it must be shielded from radiated noise as it passes from module to module. This is most easily accomplished by routing the connection away from the module on the opposite side of the printed wiring board. On the HDM and HDM+ Series converters, the minus input plane can be used to provide the necessary shielding. On the HDM-200, the $-Sense$ signal can be used to provide the necessary shielding.

Paralleling Two Converters Without Redundancy

See Figure 1 for example of paralleling (2) converters without redundancy.

At the Output

When connecting two converters in parallel, the $+V_{out}$ signals should be "hard-tied" together in a low-impedance connection. This is best accomplished by tying the signals together in a large plane of a printed wiring board. The same is true for the $-V_{out}$ signals. The $+V_{out}$ and $-V_{out}$ signals should also be routed in parallel planes in opposite layers. For example, the $+V_{out}$ load trace might be routed on layer 1 with the $-V_{out}$ load trace routed on layer 2, directly below the $+V_{out}$ trace. Also, consider using a ground shield layer within the printed wiring board to shield the load lines from potential system noise pickup.

The Sense Signals

The +Sense and –Sense signals of paralleled converters should be physically connected to the same point. That is, one paralleled converter should not have its Sense lines tied locally at its output pins, while the other paralleled module has its Sense lines connected at the load.

If employing Remote Sense (see HDMA-103 Remote Sensing), the sense lines should be tied together at the converter's pins and the +Sense and –Sense signals brought out to the load as two signals.

The Sense signals should be routed in close proximity to each other. Also, consider using a ground shield layer to shield the lines.

Paralleling with Redundancy or with Three or More Converters

When redundancy is required, or when paralleling three or more converters, an oring diode needs to be connected in series with the positive output of each paralleled converter. Solid-state relays need to be employed in the parallel pin connection and +sense pin connection. See Figure 2 for proper connection. The solid-state relays perform several functions. One is to enable the converter to start by isolating its parallel control signal from the other converters during a start-up condition. Another function is to isolate the converter's parallel signal from the other converter's parallel signal, should the converter fail. A failed converter will often have a low impedance at its parallel pin. Without a solid-state relay controlled by the converter's output, the failed converter would cause a low impedance at all of the parallel signals in the buss and redundancy would thus not be accomplished.

A zener diode is connected in series with a resistor and the diodes of the solid-state relays. This zener diode should be chosen so that the output voltage must rise to approximately 70% of its nominal level

before current starts to flow through the diodes of the solid-state relays. For example, in a system employing 12V converters, the output voltage of the converter will be about 12.5V because of the forward drop of the oring diode. 70% of 12.5V is 8.75V. The forward drop of each of the diodes of the solid-state relays is about 1.2V. $8.75V - 1.2V - 1.2V = 6.35V$. A 6.2V zener diode would be a good choice. The recommended nominal current through the diode of the solid-state relays is about 10mA. The resistor is sized to control this current and its value is calculated as follows: $R = (V_{out} - V_z - V_{relays}) / 10mA$, or $(12.5V - 6.2V - 2.4V) / 10mA = 390\Omega$. A 392Ω resistor is chosen. See Table 1 for recommended values for standard output voltages.

The oring diode is chosen for minimal forward voltage drop with minimal leakage during a fault condition. For outputs up to 20VDC, an IR p/n 112CNQ030A series diode is recommended. For outputs up to 28VDC, an IR p/n 110CNQ045A series diode is recommended.

Synchronization

The sync option may be used with paralleled modules to eliminate any beat frequency ripple that may be present at the output. Beat frequency ripple is generally not a problem with HDM modules, and low ripple is achieved without synchronization. The feature may be used to reduce ripple though, through in-phase operation (beat frequency), or through 180 degrees out-of-phase operation for an even number of units, or 120 degrees out-of-phase operation for applications where three modules are applied. More detailed information on synchronization of HDM modules is presented in a separate synchronization application note (HDMA-102.)

Trimming Paralleled Converters

Simple Fixed Trimming

Trimming paralleled converters can be accomplished several ways. The simplest method of trimming paralleled converters is to determine the desired output voltage of the paralleled converters and calculate the necessary trim resistor value as though a single converter was to be trimmed (see HDMA-104). A



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Application Note

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separate resistor would be connected between the trim and sense pin of each paralleled converter. See Figures 3 and 4.

Design Example with Adjustable Trimming

Refer to Figure 5. As an example, we will assume that a power system has the following requirements: The load voltage needs to be adjustable from 10.8V to 13.2V at a current level of about 90A. It is also a system requirement to have two (2) redundant converters in the system. A 12V HDM+ converter is selected to be used in the power system. The rating of a 12V HDM+ converter is 324W. It is desired to sense and regulate the system voltage at the cathode side of the oring diodes. It needs to be taken into account that the converters will be actually be operating at about 0.5V above the sensed voltage because the converters will be compensating for the forward drop of the oring diodes. The current rating of the converters will be reduced as to not exceed the maximum output power rating of the converter of 324W. The converters could be operating at a maximum output voltage of the upper trimmed level of 13.2V, plus the 0.5V drop of the oring diodes, or 13.7V. Upon reviewing the data sheet for the HDM+ converter, it is noted that 13.7V is beyond the 10% guaranteed minimum trim range for the converter. The factory is consulted and it is realized that it is acceptable to operate the 12V HDM+ converter at 13.7V, provided the 324W maximum power output of the converter is not exceeded. The current rating of the 12V HDM+ converter while operating at 13.7V is reduced as follows: $P_{rated} = V_{out} * I_{out}$. $324W = 13.7V * I_{out}$. Solving for I_{out} , we get $I_{out} = 23.7A$. The system need is for 90A. $90A/23.7A = 3.8$ converters. Four (4) converters will therefore be needed to provide the desired power to the load. Because we also want two redundant converters, six (6) converters will be used.

The next step is to calculate the trim resistor that would be needed to trim a 12V HDM+ converter up to 13.2V. Referring to HDMA-104 Output Voltage Trimming, a trim resistor value of 24.3kΩ is calculated and selected. The resistor is denoted as R_{vmax} . Next, the resistor needed to trim the converter down to 10.8V is calculated and selected

to be 150kΩ. The resistor is denoted as R_{vmin} . The smaller of the two resistors values is noted at 24.3k. This value will be used later and denoted as R_s . The intermediate nodal voltage is then calculated as follows:

$$V_{node} = (V_{min} - 1.5) * (R_{vmax} / R_{vmin}) + 1.5$$
$$V_{node} = (10.8 - 1.5) * (24.3k / 150k) + 1.5$$
$$V_{node} = 3.0V$$

A 25kΩ potentiometer is selected. Lastly, the top resistor (R_t) is calculated as follows:

$$R_t = \frac{(V_{min} - V_{node}) * R_{pot} * R_s / \text{number of converters}}{(V_{node} * R_s / \text{number of converters}) + (V_{node} - 1.5) * R_{pot}}$$

$$R_t = \frac{(10.8 - 3) * 25k * 24.3k / 6}{(3 * 24.3k / 6) + (3 - 1.5) * 25k}$$

$$R_t = 15.9k.$$

A standard 1% value of 15.8k is selected for R_t .

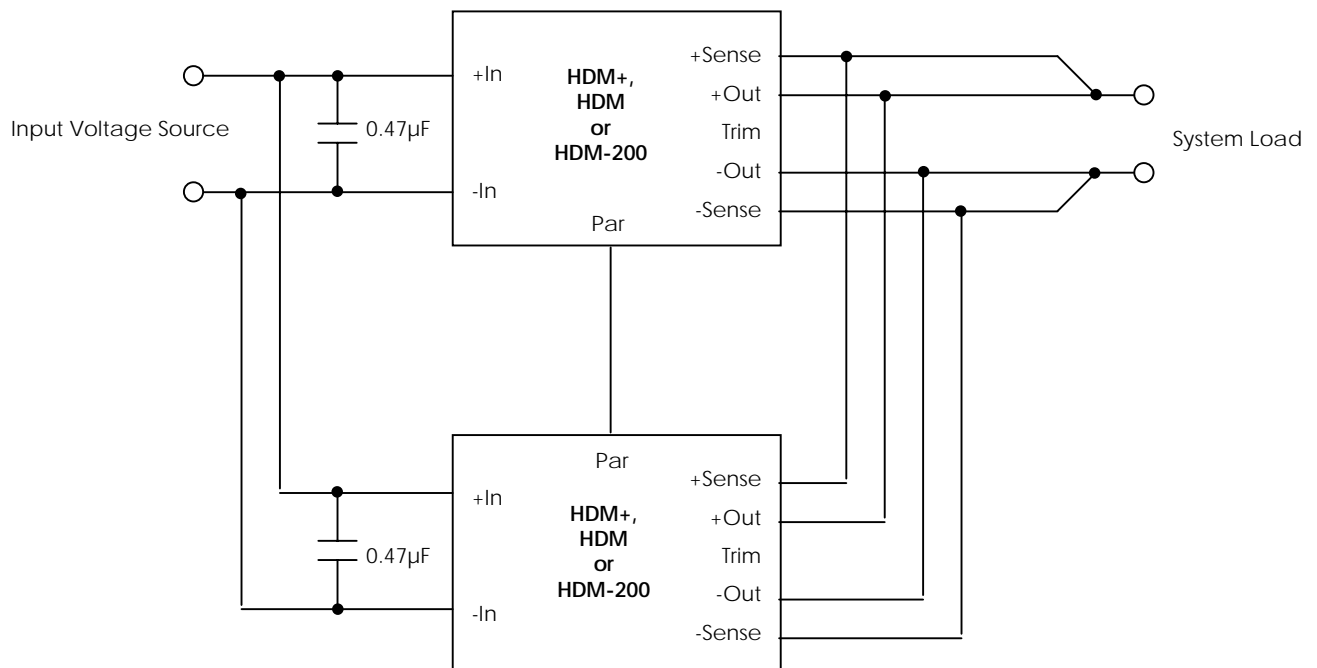


Figure 1: Parallel Connection of (2) HDM+, HDM, or HDM-200 Series Converters with No Redundancy

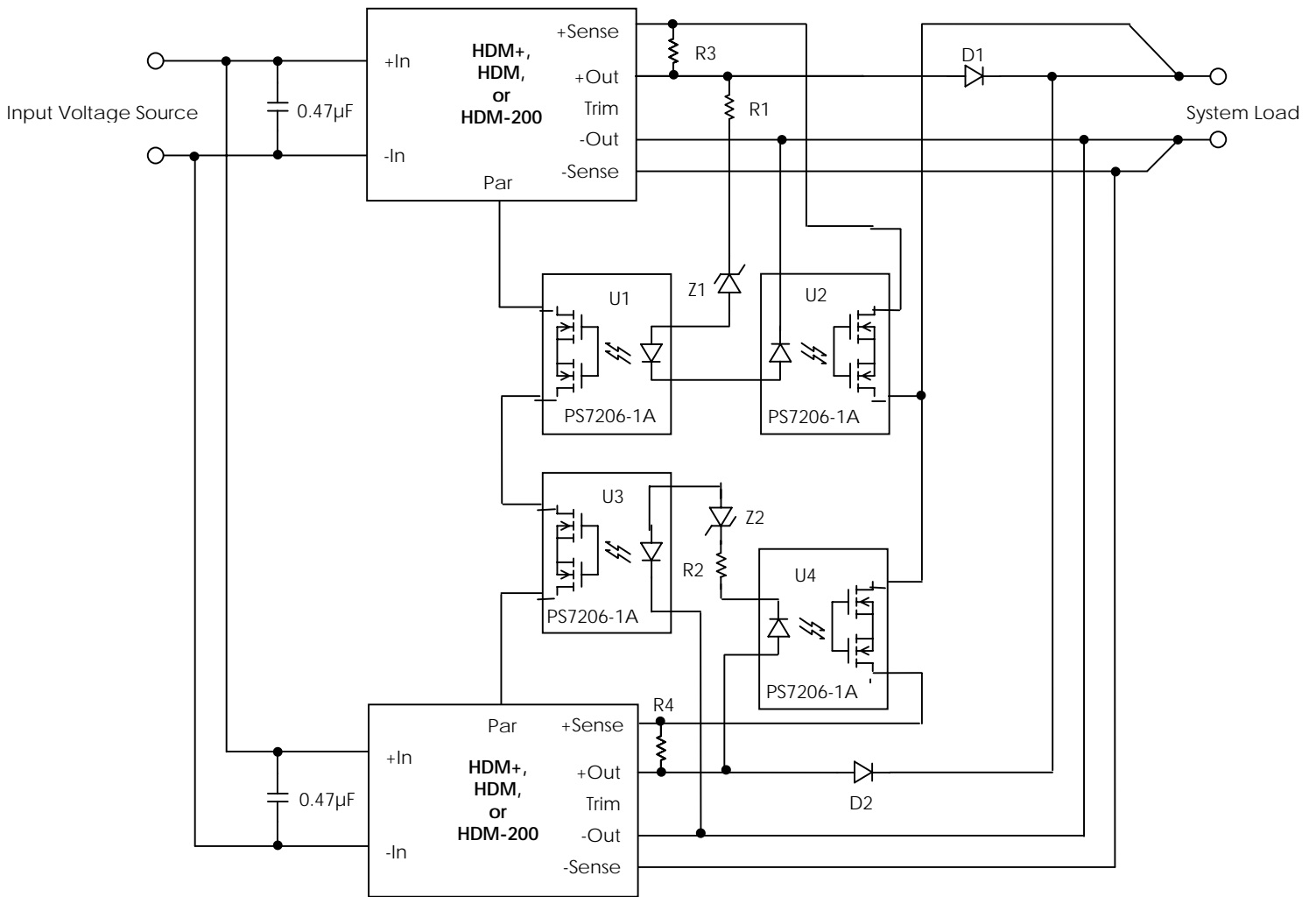


Figure 2: Parallel Connection of HDM+, HDM, or HDM-200 Series Converters with Redundancy or three (3) or more converters.

Vout	Z1,Z2	R1,R2	R3,R4	D1,D2	U1-U4
3.3V	N/A (Shorted)	127Ω / 0.125W	10Ω / 0.250W	112CNQ030A	PS7206-1A
5V	BAV303 (2x in series)	169Ω / 0.125W	10Ω / 0.250W	112CNQ030A	PS7206-1A
8V	BZM55B3V6	249Ω / 0.125W	24.9Ω / 0.250W	112CNQ030A	PS7206-1A
12V	BZM55B6V2	392Ω / 0.250W	49.9Ω / 0.250W	112CNQ030A	PS7206-1A
15V	BZM55B8V2	487Ω / 0.250W	75Ω / 0.250W	110CNQ045A	PS7206-1A
24V	BZM55B15	715Ω / 0.250W	100Ω / 0.250W	110CNQ045A	PS7206-1A

28V	BZM55B18	806Ω / 0.250W	121Ω / 0.250W	110CNQ045A	PS7206-1A
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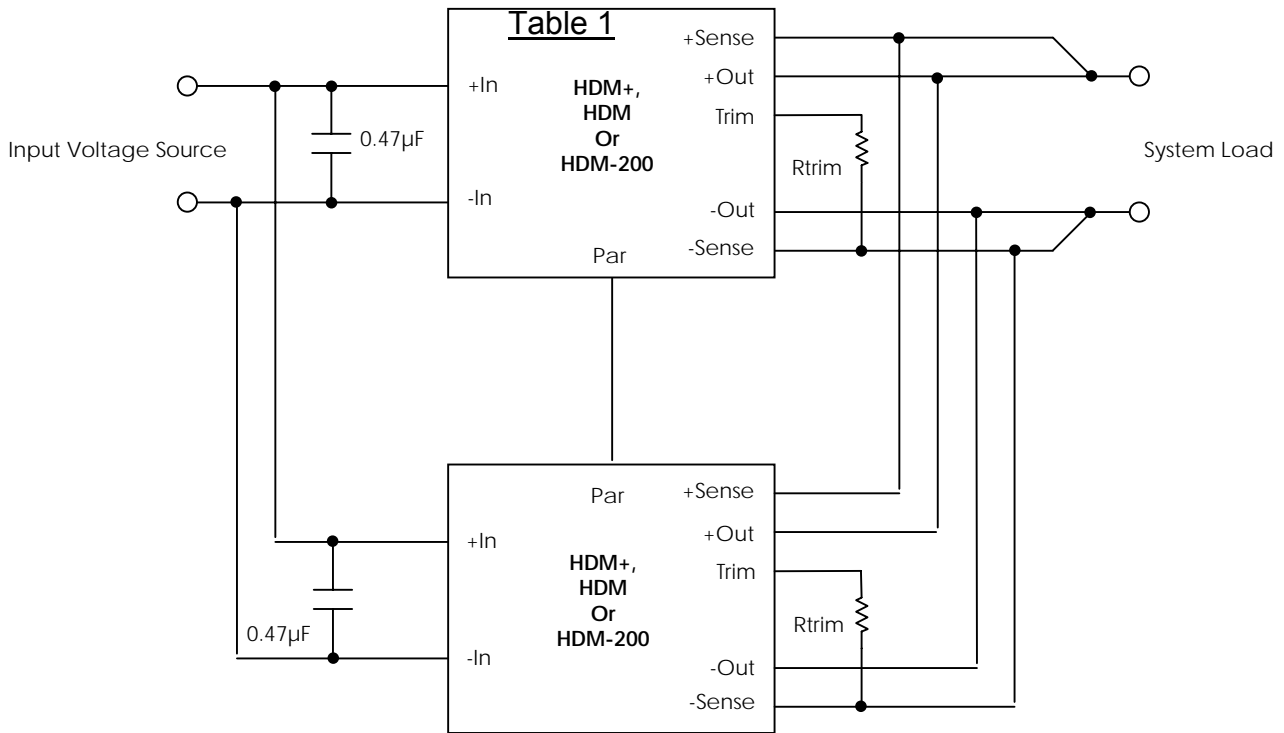


Figure 3: Parallel Connection of (2) HDM+, HDM, or HDM-200 Series Converters with Simple Trim-up

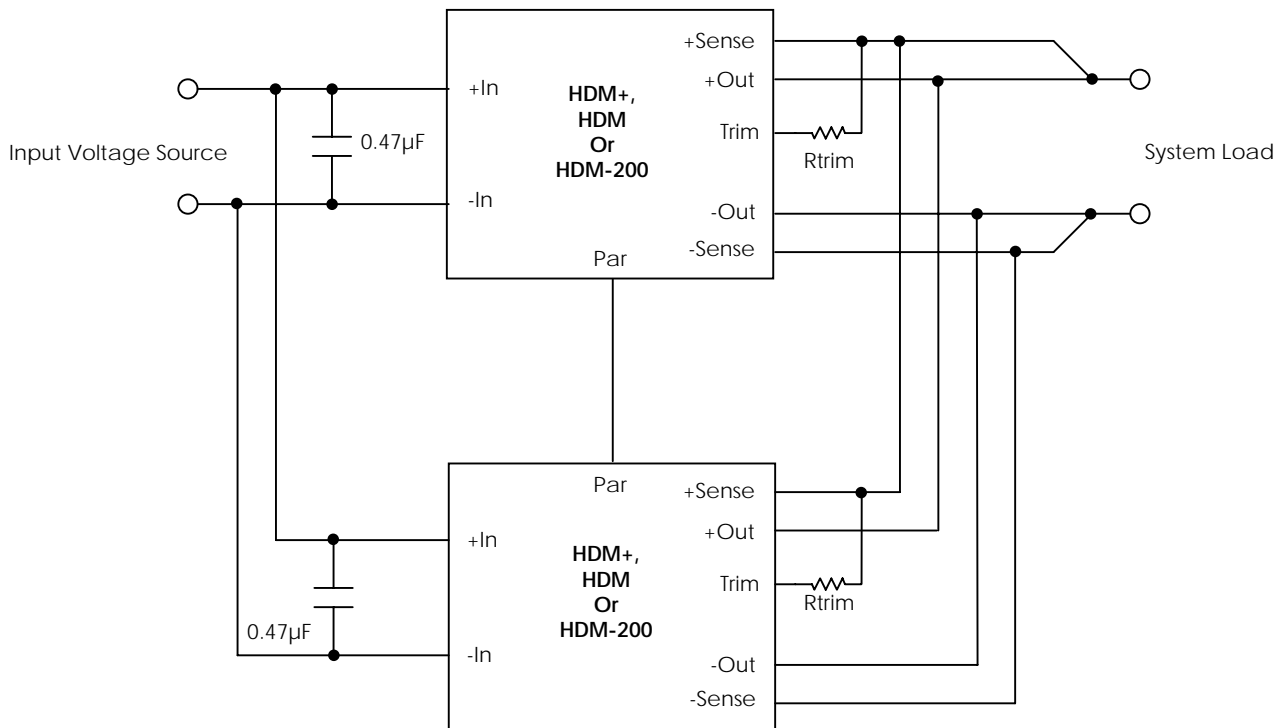


Figure 4: Parallel Connection of (2) HDM+, HDM, or HDM-200 Series Converters with Simple Trim-down

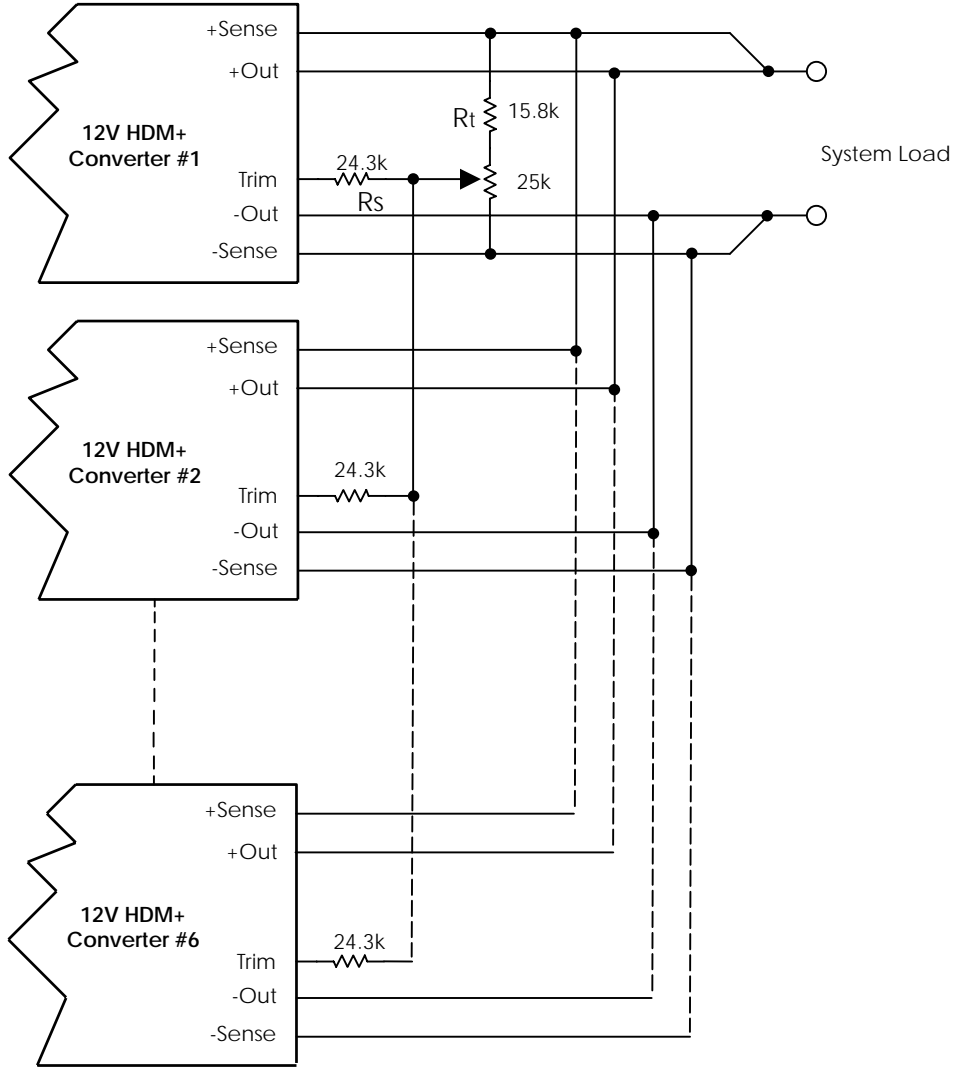


Figure 5: Parallel Connection of (6) 12V HDM+ Series Converters with Trim Network enabling user to trim up or trim down; Paralleling and Redundancy circuitry omitted for clarity.